Amendments to the Specification:

The paragraph beginning at Page 1, line 1, just above the title, is to be deleted.

A paragraph beginning at Page 1, line 5, just below the title, is to be added as follows:

Cross-Reference to Related Applications

This is a Continuation-In-Part Application of USSN 10/160,273, filed on June 4, 2002, now Issued US Patent No. 6,746,105, which is a Continuation Application of USSN 09/112,767, filed on July 10, 1998, now Issued US Patent No. 6,416,167.

The paragraphs beginning at Page 2, lines 8-21, to be amended as follows:

A silicon dioxide or glass layer 18 is positioned on the wafer substrate 14. The layer 18 defines CMOS dielectric layers. CMOS top-level metal defines a pair of aligned aluminum electrode contact layers ~~22~~ 20 positioned on the silicon dioxide layer 18. Both the silicon wafer substrate 14 and the silicon dioxide layer 18 are etched to define an ink inlet channel 22 having a circular cross section. An aluminum diffusion barrier 24 of CMOS metal 1, CMOS metal 2/3 and CMOS top level metal is positioned in the silicon dioxide layer 18 about the ink inlet channel 22. The barrier 24 serves to inhibit the diffusion of hydroxyl ions through CMOS oxide layers of the drive circuitry layer ~~11~~16.

A portion of the diffusion barrier 24 extends from the silicon dioxide layer 18. An ink passivation layer in the form of a layer of silicon nitride 26 is positioned over the aluminum contact layers 20 and the silicon dioxide layer 18, as well as the diffusion barrier 24. Each portion of the layer 26 positioned over the contact layers has an opening 28 defined therein to provide access to the contacts ~~22~~20.